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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,595	12/31/2003	Tayib Sheriff	ITL.1079US (P18343)	8595

21906 7590 02/28/2006

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EXAMINER	
FARROKH, HASHEM	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,595	SHERIFF ET AL.	
	Examiner	Art Unit	
	Hashem Farrokh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-11,18-20,22-24,26,27,29 and 30* is/are rejected.

7)☒ Claim(s) *8,12-17,21,25 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The instant application having application No. 10/750,595 has a total of 30 claims pending in the application; there are 4 independent claims and 26 dependent claims, all of which are ready for examination by the examiner.

INFORMATION CONCERNING CLAIMS:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> *A person shall be entitled to a patent unless –*
>
> *(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.*

Claims 1-7, 9-11, 18-20, 22-24, 26-27, and 29-30 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Publication No. 2003/0140244 A1 to Dahan et al. (hereinafter Dahan).

1. In regard to claim 1 Dahan teaches:

"A system **(Fig. 1)** comprising: a process comprising multiple-mapped memory;" **(e.g., see paragraph 131 in page 11; table 4; Fig. 9).**

"a first set of memory mapped onto the multiple-mapped memory **(element 311 in Fig. 4)**, a second set of memory **(element 312 in Fig. 3)** mapped onto the multiple-mapped memory;" **(e.g., see paragraph 131 in page 11; table 4; Fig. 9).** *The MPU (element*

102 in Fig. 1) is a part of the megacell (element 100 in Fig. 1), which includes the first and second set of memories.

"and an address overload circuit to selectively map the multiple-mapped memory to the first set of memory or to the second set of memory." **(e.g., see paragraphs 50-51 in page 3; paragraphs 131-134 in page 11; Figs. 2 and 9).** *The memory management units (MMUs) (elements 210 and 212 in Fig. 2) include TLBs that performs the multiple memory mapping.*

2. *In regard to claim 2 Dahan teaches:*

"wherein the second set of memory comprises instructions that are effective to execute a protected function." **(e.g., see abstract; element 416 in Fig. 4).** *For example ROM 311 shown in Fig. 4 include secure routine that* comprises instructions that are effective to execute a protected function.

3. *In regard to claim 3 Dahan teaches:*

"further comprising a transfer agent to receive parameters from the process and to assume control of execution of the process when the multiple-mapped memory is mapped to a protected set of memory."" **(e.g., see paragraph 45 in pages 2-3; element 302 in Fig. 3).** *For example the ROM 310 includes the security agent and receives the security signal 302 or parameter shown in Fig. 3.*

4. *In regard to claim 4 Dahan teaches:*

"wherein the transfer agent is effective to call a protected function." **(e.g., see paragraph 83 in page 5; Fig. 5).**

5. In regard to claim 5 Dahan teaches:

"wherein the transfer agent is effective to call the protected function using parameters received from the process." **(e.g., see paragraph 45 in pages 2-3; element 302 in Fig. 3).**

6. In regard to claim 6 Dahan teaches:

"wherein the transfer agent is stored on nonvolatile memory." **(e.g., see element 416 in Fig. 4).** *For example ROM is a non-volatile memory.*

7. In regard to claim 7 Dahan teaches:

"wherein the transfer agent executes on internal memory." **(e.g., see paragraph 40 in page 2).** *The trusted or secure code or transfer agent is stored in ROM/SRAM. Both ROM and SRAM are internal or chip memories.*

9. In regard to claim 9 Dahan teaches:

"A method **(claim 1)** comprising: executing a process that comprises multiple-mapped memory;" **(e.g., see paragraph 131 in page 11; table 4; Fig. 9).**

"determining whether the process is a trusted process;" **(e.g., see paragraph 75 in page 5; step 512 in Fig. 5).**

"if the process is determined not to be a trusted process **(e.g., see paragraph 74 in page 5; step 514 in Fig. 5)**, mapping the multiple-mapped memory to unprotected memory;" **(e.g., see paragraph 131 in page 11; elements 904 and 924 in Fig. 9).**

"and if the process is determined to be a trusted process **(e.g., see paragraph 75 in page 5; steps 520-530 in Fig. 5)**, mapping the multiple-mapped memory to protected memory." **(e.g., see paragraph 131 in page 11; element 900 in Fig. 9).**

10. In regard to claim 10 Dahan teaches:

"further comprising: storing a transfer agent." **(e.g., see element 416 in Fig. 4).**

11. In regard to claim 11 Dahan teaches:

"wherein the transfer agent is stored in a first memory." **(e.g., see element 416 in Fig. 4).** *Both ROM and SRAM include secure memory which stores the trusted code (see Fig. 9).*

18. In regard to claim 18 Dahan teaches:

"An article comprising a machine-readable storage medium on which there are stored instructions that **(see abstract)**, if executed **(see abstract; paragraph 10 in page 1)**, enable a system to:"

"determine whether a process is a trusted process;" **(e.g., see paragraph 75 in page 5; step 512 in Fig. 5).**

"and if the process is a trusted process **(step 512 in Fig. 5)**, transfer **(steps 520-526 in Fig. 5)**, at least temporarily, control of the process to a transfer agent." **(e.g., see paragraph 83 in page 5; element 416 in Fig. 4; step 542 in Fig. 5).** *I f it is determined that the process a secure or trusted process steps 520-526 is performed to set-up the security environment then at step 542 the process is transfer to security routine which is a security code stored ROM (e.g., element 416 in Fig. 4). This security code represents the transfer agent recited in the claim.*

19. In regard to claim 19 Dahan teaches:

"wherein instructions **(abstract)**, if executed **(see abstract; paragraph 10 in page 1)**, enable the system to transfer process parameters to the transfer agent." **(e.g., see paragraph 45 in pages 2-3; element 302 in Fig. 3).**

20. In regard to claim 20 Dahan teaches:

"wherein the instructions **(abstract)**, if executed **(see abstract; paragraph 10 in page 1)**, enable the system to identify and execute a protected function." **(e.g., see abstract; element 416 in Fig. 4).**

22. In regard to claim 22 Dahan teaches:

"wherein the instructions **(abstract)**, if executed **(see abstract; paragraph 10 in page 1)**, enable the system to determine whether a process is a trusted process in response to the detection of multiple-mapped memory." **(e.g., see paragraph 75 in page 5; step 512 in Fig. 5).**

23. In regard to claim 23 Dahan teaches:

"wherein the instructions **(abstract)**, if executed **(see abstract; paragraph 10 in page 1)**, enable the system to: determine that a process is a trusted process;" **(e.g., see paragraph 75 in page 5; step 512 in Fig. 5).**

"transfer, at least temporarily, control of the process to the transfer agent;" **(e.g., see paragraph 83 in page 5; element 416 in Fig. 4; step 542 in Fig. 5).**

"and transfer process parameters to the transfer agent." **(e.g., see paragraph 45 in pages 2-3; element 302 in Fig. 3).**

24. In regard to claim 24 Dahan teaches:

"wherein the instructions **(abstract)**, if executed **(see abstract; paragraph 10 in page 1)**, enable the system to: by operation of the transfer agent, identify, call, and execute a protected process." **(e.g., see paragraph 83 in page 5; Fig. 5)**

26. In regard to claim 26 Dahan teaches:

"A system **(Fig. 1)** comprising: an integrated circuit device **(paragraph 169 in page 14; element 100 in Fig. 1)** comprising a processor **(element 102 in Fig. 1)**, internal random access memory (RAM) **(element 312 in Fig. 3)**, and internal read only memory (ROM);" **(element 311 in Fig. 3).** *Fig. 3 is a block diagram of MPU 102 within the megacell 100 which is an integrated circuit and includes SRAM and ROM.*

"unprotected memory;" **(elements 311 and 313 in Fig. 3).** *Both SRAM and ROM include public or unprotected memories.*

"protected memory;" **(elements 310 and 312 in Fig. 3).** *Both SRAM and ROM include secure or protected memories.*

"a process to execute on the internal RAM **(paragraph 46 in page 3)**, the process comprising multiple-mapped memory **(Fig. 9)**, the multiple-mapped memory to be selectively mapped to either the protected memory or the unprotected memory;" **(e.g., see claim 3).** *Dahan teaches that TLB has entries for both secure and unsecured mapping of virtual to physical address. Depending on mode of operation (e.g. Fig. 5) one of the translation or mapping to secure or unsecured inherently is selected.*

"a trust co-processor to determine whether the multiple-mapped memory is to be mapped to the unprotected memory or is to be mapped to the protected memory;" **(e.g., see paragraph 47 in page 3; element 150 in Fig. 1)**. *For example Security State Machine (SSM) represent the co-processor stated in the claim.*

"a wireless interface coupled to the processor;" **(e.g., see paragraph 166 in page 14; element 18 in Fig. 12).**

"and an antenna coupled to the wireless interface." **(e.g., see paragraph 166 in page 14; element 18 in Fig. 12).** *Dahan teaches the wireless for use in communicating with other user's of wireless network. Therefore, the wireless link disclosed inherently must be coupled to an antenna.*

27. In regard to claim 27 Dahan teaches:

"further comprising a circuit coupled to the trust co-processor to selectively map the multiple-mapped memory to the protected memory." **(e.g., see paragraph 54 in page 3; elements 210 AND 300 in Fig. 3).** *The MMU 210 is used for mapping the logical or virtual address to multiple mapped memories. Fig 3 shows that MMU is coupled to the SSM (element 300) through various signals.*

29. In regard to claim 29 Dahan teaches:

"further comprising a transfer agent to receive parameters from a trusted process **(e.g., see paragraph 45 in pages 2-3; element 302 in Fig. 3)**, call a protected function using the parameters, and cause the protected function to execute."

30. In regard to claim 30 Dahan teaches:

"further comprising a circuit coupled to the trust co-processor to selectively map the multiple-mapped memory to the protected memory." **(e.g., see paragraph 54 in page 3; elements 210 AND 300 in Fig. 3).** *The MMU 210 is used for mapping the logical or virtual address to multiple mapped memories. Fig 3 shows that MMU is coupled to the SSM (element 300) through various signals.*

ALLOWABLE SUBJECT MATTER

Claims 8, 12-17, 21, 25, and 28 are objected to as being dependent upon rejected based claims, but would be allowable if rewritten in correct and independent form including all of the limitations of the base claim and any intervening claims.

1. The primary reason for allowance of claims 8 and 28 in instant application is the combination with the inclusion of the following limitations: **wherein the address overload circuit comprises: (a) an address multiplexer; (b) an address translator coupled to the address multiplexer**

"and (c) a data multiplexer."

2. The primary reason for allowance of claims 12-17 in instant application is the combination with the inclusion of the following limitations: **copying the transfer agent to a second memory; transferring parameters from the process to the transfer agent**

3. The primary reason for allowance of claims 21 and 25 in instant application is the combination with the inclusion of the following limitations: **wherein the instructions, if executed, enable the system to copy the transfer agent from nonvolatile memory to volatile memory in the course of executing multiple-mapped memory**

: IMPORTANT NOTE :

I f the applicant should choose to rewrite the independent claims to include the limitations recited in either one of the claims, the applicant is encouraged to ***amend the***

title of the invention *such that it is descriptive of the invention as claimed as required be sec.* ***606.01*** *of the* ***MPEP****. Furthermore, the* ***summary of invention*** *and the* ***abstract*** *should be amended to bring them into harmony with the allowed claims as required by paragraph 2 of* ***sec. 1302.01*** *of the* ***MPEP****.*

As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not compiled with. See ***37 C.F.R. § 1.111(b)*** *and* ***§ 707.07(a) of the M.P.E.P.***

Conclusion

The prior art made of record and not relied upon are as follows:

1. *U. S. Patent No. 6,606,707 B1 to Hirota et al. Semiconductor memory card.*
2. *U. S. Patent Publication No. 2005/0055524 A1 to* Gulick *et al. describes Computer system employing a trusted execution environment including a memory controller configured to clear memory.*
3. *U. S. Patent No. 6,775,750 B2 to* Krueger *describes System protection map.*

Any inquiry concerning this communication should be directed to Hashem Farrokh whose telephone number is (571) 272-4193. The examiner can normally be reached Monday-Friday from ***8:00 AM to 5:00 PM.***

If attempt to reach the above noted Examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Donald A Sparks, can be reached on (571) 272-4201. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published

application may be obtained from either private PAIR or Public PAIR. Status information for unpublished application is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBS) at 866-217-9197 (toll-free).

HF

HF

2006-02-20

DONALD SPARKS
SUPERVISORY PATENT EXAMINER